Module Overview

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- high-speed counter module overview
- operating modes
- hardware features

High-Speed Counter Module Overview

The High-Speed Counter Module, catalog number 1746-HSCE is an SLC 500 family compatible device except with the 1747-ASB Remote I/O Adapter Module. The high-speed module can be used with SLC 5/02 (and above) processors.

The module's bidirectional counting ability allows it to detect movement in either direction. In addition, x2 and x4 counting modes are provided to fully use the capabilities of high resolution quadrature encoders.

High-speed inputs from quadrature encoders and various high-speed switches are supported. Accepting input pulse frequencies of up to 50k Hz allows precise control of fast motions.

In addition to providing an Accumulated Counter, the module provides a Rate Counter to determine Rate Measurement by indicating the pulse input frequency in Hz. (Refer to the block diagram on the following page.) The Rate Measurement is determined by accumulating input pulses over a fixed period of time. You set the Rate Period to best match your application requirements.

Background Rate calculation is provided in Sequencer and Range Modes. This operation accepts input rates up to 32,767 Hz. The dynamically configurable Rate Period ranges from 10 ms to 2.55 seconds.

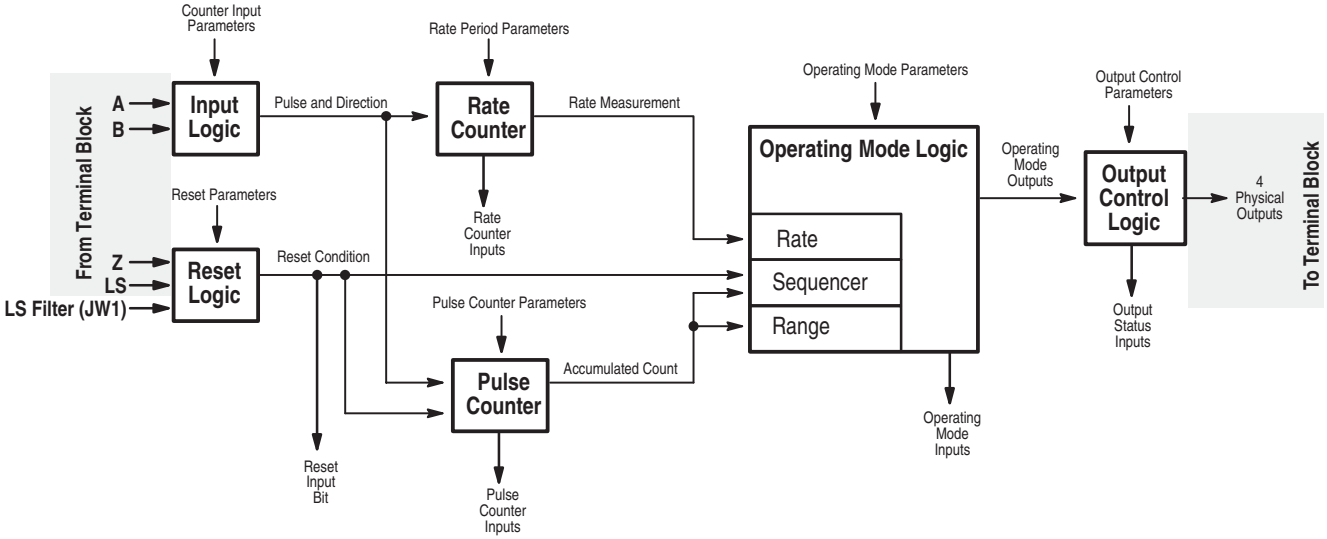
The module's four current sink (open collector) outputs can be controlled from one of two sources:

- the user program
- the module

Control of the counter reset is configured through user-set parameters. The counter can be reset from any combination of the Z input, Limit Switch input, or Soft Reset control bits.

Module operation is determined by selections made in the Setup and Control Word (M0:e.1). Setting the Function Control bit to 1 triggers the module to start the proper pulse counter, rate measurement, and output control functions. Many parameters are dynamic and can be changed without disrupting counter operation.

A block diagram of the module is shown below. Inputs from the terminal block enter the diagram at the left, outputs to the terminal block exit at the right. M0 and Output file parameters from the SLC enter the logic blocks from the top. Input file data to the SLC exit the logic blocks from the bottom.



Counter Input Parameters
- Input Type (M0:e.1/9–11)
- Up/Down Count Direction (M0:e.1/3) *–d*

Reset Parameters
- Soft Reset bit (M0:e.1/4) *–d*
- Reset Mode (M0:e.1/5–7)

Rate Period Parameters
- Rate Period (M0:e.9/0–7 or M0:e.16/0–7) *–d*

Operating Mode Parameters
- Operating Mode (M0:e.1/14–15)
- Function Control Bit (M0:e.1/12)
- Range Definitions:
  - Range Starting Values (M0:e.10 – 33) *–d*
  - Range Ending Values (M0:e.10 – 33) *–d*
  - Range Outputs (M0:e.3 – 8) *–d*
  - Valid Ranges (M0:e.2) *–d*
- Sequencer Definitions:
  - Valid Steps (M0:e.2 and M0:e.3/0–7) *–d*
  - Step Presets (M0:e.17 – 40) *–d*
  - Step Outputs (M0:e.4 – 15) *–d*
  - Initial Outputs (M0:e.3/8–15) *–d*
  - Sequencer Reset (M0:e.1/0) *–d*

Pulse Counter Parameters
- Reset Value (M0:e.34 or M0:e.41) *–d*
- Maximum Count Value (M0:e.34 or M0:e.41)
- Counter Hold bit (M0:e.1/2) *–d*
- Counter Type bit (M0:e.1/13)

Output Control Parameters
- Direct Outputs (O:e.0/0–7) *–d*
- Output Source Select (M0:e.0/0–7) *–d*
- Enable Outputs bit (M0:e.1/1) *–d*

Rate Counter Inputs
- Rate Valid (I:e.0/3)
- Rate Counter Overflow (I:e.0/4)
- Rate Measurement Overflow (I:e.0/5)
- Zero Rate Period Count (I:e.0/2)
- Rate Period Count (I:e.2)
- Rate Measurement (I:e.3)

Pulse Counter Inputs
- Accumulated Count (I:e.1)
- Overflow/Underflow (I:e.0/13)
- Pulse Counter State (I:e.0/14–15)

Reset Input bit (I:e.0/12)

Operating Mode Inputs
- Sequencer Inputs
  - Current Sequencer Step (I:e.5/0–7)
  - Next Sequencer Step (I:e.5/8–15)
  - Sequence Done (I:e.0/6)
- Range inputs
  - Ranges Active (I:e.6/0–11)

Output Status Inputs (I:e.4/8–15)

Error Inputs
- Critical Error (I:e.0/10)
- Configuration Error bit (I:e.0/11)
- Configuration Error Code (I:e.4/0–7)

–d indicates a dynamic parameter